REMARKS

Claims 1-42 are pending in the application.

Claims 1 and 22 are rejected.

Claims 2-21 and 23-42 are objected to as depending from a rejected base claim, but are allowable if written in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2 and 23 have been rewritten in independent form as suggested by the Examiner. Claims 2-21 and 24-42 are now dependent from independent claims with allowable material.

I. REJECTION UNDER 35 U.S.C. § 102(b)

The Examiner rejected Claim 1 under *35 U.S.C. §102(b)* as being anticipated by U.S. Patent No. 6,288,564 to *Hedberg* (hereafter "*Hedberg*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Independent Claim 1 is directed to a receiver circuit for terminating a transmission line. The receiver circuit comprises a receiver having an input coupled to a transmission line output of said transmission line forming a common node, an output generating a digital signal in response to a signal at said transmission line output and a threshold voltage, a termination network coupled to said common node for setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals, and logic circuitry for generating said plurality of control signals in response to a plurality of mode setting inputs. The Examiner states that *Hedberg* teaches

all the claimed features of Claim 1 and cites Fig. 1. The Examiner states that receiver 1 of *Hedberg* has "an input (IN) coupled to a transmission line (TR) forming the common node (as the node connecting the output of the transmission line and the input of the receiver, not marked, an output generating a digital signal (OUT) in response to a signal (IN) at said transmission line output and a threshold voltage (a voltage from 2); a termination network (2) coupled to said common node for setting a plurality of Thevenins voltages (TZ1-TZ3) and Thevenins impedances (resistance of TZ1-TZ3) in response to a plurality of control signals (outputs of A1-A3); and logic circuitry (3) for generating said plurality of control signals in response to a plurality of mode setting inputs (input signals provided by A1-A2)."

While receiver (1) of *Hedberg* has in input (IN) coupled to TR, the output of receiver (1) is only generated in response to a signal received at IN. Nowhere does *Hedberg* show a threshold voltage. Also, contrary to the Examiner's assertion, element (2) does not provide a voltage (Thevenins voltage cited in Claim 1). The three devices TZ1-TZ3 only provide an impedance level at the input (IN). The Examiner states that *Hedberg* teaches a termination network (2) coupled to the common node for setting a plurality of Thevenins voltages (TZ1-TZ3) and Thevenins impedances (TZ1-TZ3). Again, element (2) of *Hedberg* does not provide any voltage and thus is not a Thevenins termination network with a Thevenins impedance and a Thevenins voltage. Element (3) is not logic circuitry, but rather is three Operation Amplifiers (A1-A3) which constitutes analog circuitry. See *Hedberg*, column 4, lines 16-18, lines 22-30, and column 5, lines 14-19. While each output of Operational Amplifiers A1-A3 is coupled to a gate of one of field effect transistors (FETS) TZ1-TZ3, these outputs are not generated in response to a plurality of mode setting signals as recited in Claim 1 of the present invention. Amplifiers A1-A3 all have their negative inputs coupled to the voltage across resistor Rref and their positive inputs coupled to the voltage across the parallel combination of FETS NZ1-NZ3. The voltage across Rref is determined by current I1 and the voltage across NZ1-NZ3 is determined by current I2. This circuitry of *Hedberg* is used to force the combination of TZ1-TZ3 to have the same impedance as NZ1-NZ3 when conducting

a current I2. The logic circuitry of Claim 1 of the present invention generates the plurality of control signals in response to a plurality of mode setting signals. The Applicant asserts that *Hedberg* does not teach or suggest setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals generated by logic circuitry in response to a plurality of mode setting signals.

Therefore, the Applicant asserts that the rejection of Claim 1 under *35 U.S.C. §102(b)* as being anticipated by *Hedberg* is traversed by the above arguments.

II. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claim 22 under *35 U.S.C. §103(a)* as being unpatentable over U.S. Patent No. 6,347,350 to *Muljono* (hereafter "*Muljono*") in view of *Hedberg*.

To establish a *prima facie* case of obviousness, the Examiner must meet three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

Claim 22 is directed to a data processing system with interface circuitry that has a receiver circuit according to the invention of Claim 1. The Examiner states that *Muljono* teaches all the claimed features of the integrated circuit (IC) recited in Claim 22, with the exception of the claimed details of the receiver circuit recited in Claim 1. The Examiner repeats his argument asserting that *Hedberg* teaches the invention of Claim 1. The Applicant has shown that *Hedberg* does not anticipate the invention of Claim 1. The Examiner makes no assertion that *Muljono* teaches or suggests the invention of Claim 1. Neither *Muljono* nor *Hedberg* teaches or suggests the limitations of Claim 1; therefore, the Applicant asserts that neither *Muljono* nor *Hedberg*, singly or in combination, teach or suggest the invention of Claim 22 which recites a data processing system including the limitation of a receiver circuit recited in Claim 1. Therefore, the Applicants respectfully

assert that the rejection of Claim 22 under *35 U.S.C. §103(a)* as being unpatentable over *Muljono* in view of *Hedberg* is traversed by the above arguments and for the same reasons argued relative to Claim 1.

III. CONCLUSION

The Applicant has traversed the rejection of Claim 1 under *35 U.S.C. §102(b)* as being anticipated by *Hedberg*.

The Applicant has traversed the rejection of Claim 22 under *35 U.S.C. §103(a)* as being unpatentable over *Muljono* in view of *Hedberg*.

Claims 2 and 23 have been rewritten in independent form to traverse the objections of Claims 2-21 and 23-42 depending from rejected claims.

The Applicants, therefore, respectfully assert that Claims 1, 3-21, 22, 24-42 and amended claims 2 and 23 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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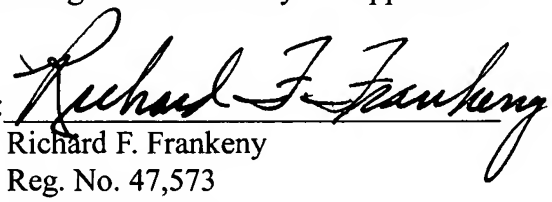
Patent Agent and Attorney for Applicants

By: 

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